CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor chip;

a first projected electrode array projecting from and disposed on a surface of the semiconductor chip, the first projected electrode array including a plurality of first projected electrodes each having a first center disposed on a first line linking the first centers; and

a second projected electrode array projecting from and disposed on the surface of the semiconductor chip, the second projected electrode array including a plurality of a second projected electrodes each having a second center disposed on a second line linking the second centers, wherein:

the first line and the second line are laterally spaced apart;

a width of each first projected electrode is smaller than a width of each second projected electrode; and

a length of each first projected electrode is longer than a length of each second projected electrode.

2. The semiconductor device according to Claim 1, wherein each first projected electrode and each second projected electrode are substantially equal to each in a surface area facing a wiring board.

3. The semiconductor device according to Claim 1, further comprising:

a wiring board on which the semiconductor chip is mounted; and

a wiring pattern connected to the first and the second projected electrodes and disposed on the wiring board.

4. The semiconductor device according to Claim 3, wherein a resin layer is provided between the semiconductor chip and the wiring board.

5. An electronic device comprising:

an electronic component;

a first projected electrode array projecting from and disposed on a surface of the electronic component, the first projected electrode array including a plurality of first projected electrodes each having a first center disposed on a first line linking the first centers; and

a second projected electrode array projected from and disposed on the surface of the electronic component, the second projected electrode array including a plurality of second projected electrodes each having a second center disposed on a second line linking the second centers, wherein:

the first line and the second line are laterally spaced apart;

a width of each first projected electrode is smaller than a width of each second projected electrode; and

a length of each first projected electrode is longer than a length of each second projected electrode.

6. Electronic equipment comprising:

a semiconductor chip;

a wiring board including a wiring pattern electrically connected to the semiconductor chip;

an electronic component electrically connected to the semiconductor chip through the wiring board;

a first projected electrode array disposed between the semiconductor chip and the wiring board, the first projected electrode array including a plurality of first projected electrodes each having a first center disposed on a first line linking the first centers; and

a second projected electrode array disposed between the semiconductor chip and the wiring board, the second projected electrode array including a plurality of second projected electrodes each having a second center disposed on a second line linking the second centers, wherein:

the first line and the second line are laterally spaced apart;

a width of each first projected electrode is smaller than a width of each second projected electrode; and

a length of each first projected electrode is longer than a length of each second projected electrode.

7. A method of manufacturing a semiconductor device that includes first and second projected electrode arrays projecting from and disposed on a semiconductor chip, the method comprising:

providing the first projected electrode array by disposing a plurality

of first projected electrodes on the semiconductor chip, each first projected electrode having a first center disposed on a first line linking the first centers;

providing the second projected electrode array by disposing a plurality of second projected electrodes on the semiconductor chip, each second projected electrode having a second center disposed on a second line linking the second centers;

mounting the semiconductor chip on a wiring board where a wiring pattern is disposed through the first and second projected electrode arrays; and

electrically connecting the wiring pattern to the first and the second projected electrode arrays;

wherein a width of each first projected electrode is smaller than a width of each second projected electrode and a length of each first projected electrode is longer than a length of each second projected electrode.